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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,074	06/26/2000	TOSHIYUKI NAKAGAWA	450101-02031	7488

20999 7590 03/26/2004

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EXAMINER	
PATHAK, SUDHANSHU C	

ART UNIT	PAPER NUMBER
2634	8

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/530,074	NAKAGAWA ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Feburary 25th, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *June 26th, 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-to-14 are pending in the application.

Response to Amendment

2. The indicated allowability of claim 2 is withdrawn in view of the newly discovered reference(s) to Szczutkowski et al. (4,817,146). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 6, 7, 9 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable by Ino et al. (5,506,581) in view of Szczutkowski et al. (4,817,146).

Regarding to Claim 1, Ino discloses a data-modulating apparatus (Fig. 1) comprising an encoding circuit (Fig. 1, element 11), a pattern generating circuit (Fig. 1, element 12). The encoding circuit translates the sequence of input data into the coded data (Column 6, lines 66-67), in accordance with the coding suited to the transmission or recording (Column 7, lines 1-2). The apparatus further comprises a pattern inserting circuit (Fig. 1, element 13) for inserting patterns at arbitrary positions of the coded data (Column 8, lines 60-68). The patterns consisting of "Tdc" bits are inserted into the coded data at the pre-set intervals "Tcode" (Column 9, lines 49-56 & Fig. 2). This may yield adding a pattern after the minimum run or a

pattern that breaks the maximum run, so as not to break the coding rule (Column 9, lines 58-67 & Column 13, lines 49-67). However, Ino does not disclose the sync pattern that breaks the maximum run is repeated twice continuously.

Szczutkowski discloses a method and apparatus for encoding / decoding data providing enhanced synchronization to provide successfully late entry synchronization (or to re-establish synchronization once lost) into an ongoing received data signal (Abstract, lines 1-13). Szczutkowski further discloses continuously repeating the synchronization pattern to ensure the synchronization acquisition (Column 16, lines 35-55 & Column 19, lines 1-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Szczutkowski teaches that repeating the synchronization pattern provides increased reliability to detect the sync pattern and thus repeating the sync pattern as described in Szczutkowski in the apparatus as described in Ino increases the reliability of synchronization of the received train of data during the maximum run.

Regarding to Claim 3, Ino in view of Szczutkowski describes a data modulating apparatus for receiving a train of data comprising a sync pattern, repeated twice continuously, that breaks the maximum run as described above. Ino further discloses data-modulating apparatus for modulating information data comprising plurality of pattern signals (Column 19, Claim 2). Ino further discloses an embodiment to the invention as consisting in that patterns comprise three different patterns (Column 2, lines 30-40). Ino further describes these inserting patterns (Column 9, lines 29-34). Therefore, it would have been obvious to one of ordinary

skill in the art at the time of the invention that Ino in view of Szczutkowski satisfies the limitations of the claim.

Regarding to Claim 4, Ino in view of Szczutkowski describes a data modulating apparatus for receiving a train of data comprising a sync pattern, repeated twice continuously, that breaks the maximum run as described above. Ino discloses an embodiment to the invention as consisting in that patterns comprise three different patterns (Column 2, lines 30-40). Ino further describes these inserting patterns to differ from each other at two or more bits when the sync patterns are detected (Column 9, lines 25-34). This thus satisfies the limitation of the claim that the sync patterns are selected such that a detection distance of 2 or more provided between the two or more patterns. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Ino in view of Szczutkowski satisfies the limitations of the claim.

Regarding to Claim 6, Ino in view of Szczutkowski describes a data modulating apparatus for receiving a train of data comprising a sync pattern, repeated twice continuously, that breaks the maximum run as described above. Ino further discloses the sync patterns are interchangeable and the selection of the pattern is by an algorithm (Column 9, lines 15-22). Ino also describes that the selection of the pattern is such that the absolute value of the sum or the digital sum value (DSV) of the modulated coded data is minimized (Column 9, lines 23-34 & Column 10, lines 15-21 & Column 11, lines 10-20). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of the invention that Ino in view of Szczutkowski satisfies the limitations of the claim.

Regarding to Claim 7, Ino discloses a data-modulating method (Fig. 1) comprising an encoding circuit (Fig. 1, element 11), a pattern generating circuit (Fig. 1, element 12). The encoding circuit translates the sequence of input data into the coded data (Column 6, lines 66-67), in accordance with the coding suited to the transmission or recording (Column 7, lines 1-2). The method further comprises a pattern inserting circuit (Fig. 1, element 13) for inserting patterns at arbitrary positions of the coded data (Column 8, lines 60-68). The patterns consisting of "Tdc" bits are inserted into the coded data at the pre-set intervals "Tcode" (Column 9, lines 49-56 & Fig. 2). This may yield adding a pattern after the minimum run or a pattern that breaks the maximum run, so as not to break the coding rule (Column 9, lines 58-67 & Column 13, lines 49-67 & Column 19, Claim 3). However, Ino does not disclose the sync pattern that breaks the maximum run is repeated twice continuously.

Szczutkowski discloses a method and apparatus for encoding / decoding data providing enhanced synchronization to provide successfully late entry synchronization (or to re-establish synchronization once lost) into an ongoing received data signal (Abstract, lines 1-13). Szczutkowski further discloses continuously repeating the synchronization pattern to ensure the synchronization acquisition (Column 16, lines 35-55 & Column 19, lines 1-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that

Szczutkowski teaches that repeating the synchronization pattern provides increased reliability to detect the sync pattern and thus repeating the sync pattern as described in Szczutkowski in the apparatus as described in Ino increases the reliability of synchronization of the received train of data during the maximum run.

Regarding to Claims 9 &10 (apparatus and method), Ino discloses a data-demodulating apparatus and method (Fig. 5) comprising a sync signal detecting means for detecting, from a train of codes, a sync signal (Fig. 5, element 24). The sync signal pattern for inserted at arbitrary positions of the coded data (Column 8, lines 60-68). The patterns consisting of "Tdc" bits are inserted into the coded data at the pre-set intervals "Tcode" (Column 9, lines 49-56 & Fig. 2). The sync patterns can be inserted that breaks the maximum run, after detecting the minimum run, depending on the value of "Tdc" and "Tcode" which are selected by (Column 9, Equation 1,2 & 3). However, Ino does not disclose the sync pattern that breaks the maximum run is repeated twice continuously.

Szczutkowski discloses a method and apparatus for encoding / decoding data providing enhanced synchronization to provide successfully late entry synchronization (or to re-establish synchronization once lost) into an ongoing received data signal (Abstract, lines 1-13). Szczutkowski further discloses continuously repeating the synchronization pattern to ensure the synchronization acquisition (Column 16, lines 35-55 & Column 19, lines 1-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Szczutkowski teaches that repeating the synchronization pattern provides increased

reliability to detect the sync pattern and thus repeating the sync pattern as described in Szczutkowski in the apparatus as described in Ino increases the reliability of synchronization of the received train of data during the maximum run.

5. Claims 8 & 11, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ino et al. (5,506,581) in view of Szczutkowski et al. (4,817,146) in further view of Kojima et al. (EP 0 779 623 A2).

Regarding to Claims 8 & 11, Ino discloses a data-modulating method and apparatus (Fig. 1) comprising an encoding circuit (Fig. 1, element 11), a pattern generating circuit (Fig. 1, element 12), pattern insertion circuit (Fig. 1, element 13), and a NRZI modulation circuit (Fig. 1, element 14), as described above. Ino further discloses, a data-demodulating method and apparatus (Fig. 5), comprising a decoding circuit (Fig. 5, element 23), a sync detection circuit (Fig. 5, element 24), and a pattern removal circuit (Fig. 5, element 22). However, Ino does not specify that the sync pattern that breaks the maximum run is repeated twice continuously.

Szczutkowski discloses a method and apparatus for encoding / decoding data providing enhanced synchronization to provide successfully late entry synchronization (or to re-establish synchronization once lost) into an ongoing received data signal (Abstract, lines 1-13). Szczutkowski further discloses continuously repeating the synchronization pattern to ensure the synchronization acquisition (Column 16, lines 35-55 & Column 19, lines 1-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Szczutkowski teaches that repeating the synchronization pattern provides increased

reliability to detect the sync pattern and thus repeating the sync pattern as described in Szczutkowski in the apparatus as described in Ino increases the reliability of synchronization of the received train of data during the maximum run. However, Ino in view of Szczutkowski does not specify a data-providing medium for providing a data modulating/demodulating apparatus with a computer-readable program.

Kojima discloses a CPU (central processing unit) and a memory to be included in the synthesizing circuit (Page 4, lines 30-32 & Fig. 1, element 30). The CPU implements an algorithm (Fig. 7) in the form of a computer program, while providing the sync pattern stored in the memory of the CPU. The CPU selects the stored pattern, which is optimum for the DC suppression from the memory as implemented in the algorithm. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the pattern generation circuit in Ino in view of Szczutkowski can be implemented by a CPU and memory unit as described in Kojima. This would provide a more compact and flexible solution for varying the pattern generation and encoding algorithm depending on the information transmitting or recording the information on a recording medium, such as magnetic tape, optical disc.

6. Claims 12 & 13, are rejected under 35 U.S.C. 103(a) as being unpatentable by Ino et al. (5,506,581) in view of Applicant Admitted Prior Art (AAPA).

Regarding to Claim 12, Ino discloses a data-modulating apparatus (Fig. 1) comprising an encoding circuit (Fig. 1, element 11), a pattern generating circuit (Fig. 1, element 12). The encoding circuit translates the sequence of input data into the

coded data (Column 6, lines 66-67), in accordance with the coding suited to the transmission or recording (Column 7, lines 1-2). The apparatus further comprises a pattern inserting circuit (Fig. 1, element 13) for inserting patterns at arbitrary positions of the coded data (Column 8, lines 60-68). The patterns consisting of "Tdc" bits are inserted into the coded data at the pre-set intervals "Tcode" (Column 9, lines 49-56 & Fig. 2). This may yield adding a pattern after the minimum run or a pattern that breaks the maximum run, so as not to break the coding rule (Column 9, lines 58-67 & Column 13, lines 49-67). However, Ino does not disclose the sync signal having six channel bits for identifying each sync signal.

The Applicant Admitted Prior Art (AAPA) discloses a data code satisfying the minimum and maximum run lengths depending on the RLL coding scheme further comprising code with six channel bits (Specification, Page 3, Table 1 "i = 2 & Specification, Page 4, lines 1-7 & Specification, Page 5, Table 2 "i = 2 & Specification, Page 6, lines 1-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing the sync pattern to contain six channel bits is a matter of design choice so as to provide a multiple of sync bits equal to the data train code bits, there is no criticality in selecting the sync pattern to have six channel bits, these could be selected depending on the application of the modulating apparatus.

Regarding to Claim 13, Ino discloses a data-modulating method (Fig. 1) comprising an encoding circuit (Fig. 1, element 11), a pattern generating circuit (Fig. 1, element 12). The encoding circuit translates the sequence of input data into the

coded data (Column 6, lines 66-67), in accordance with the coding suited to the transmission or recording (Column 7, lines 1-2). The method further comprises a pattern inserting circuit (Fig. 1, element 13) for inserting patterns at arbitrary positions of the coded data (Column 8, lines 60-68). The patterns consisting of "Tdc" bits are inserted into the coded data at the pre-set intervals "Tcode" (Column 9, lines 49-56 & Fig. 2). This may yield adding a pattern after the minimum run or a pattern that breaks the maximum run, so as not to break the coding rule (Column 9, lines 58-67 & Column 13, lines 49-67 & Column 19, Claim 3). However, Ino does not disclose the sync signal having six channel bits for identifying each sync signal.

The Applicant Admitted Prior Art (AAPA) discloses a data code satisfying the minimum and maximum run lengths depending on the RLL coding scheme further comprising code with six channel bits (Specification, Page 3, Table 1 "i = 2 & Specification, Page 4, lines 1-7 & Specification, Page 5, Table 2 "i = 2 & Specification, Page 6, lines 1-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing the sync pattern to contain six channel bits is a matter of design choice so as to provide a multiple of sync bits equal to the data train code bits, there is no criticality in selecting the sync pattern to have six channel bits, these could be selected depending on the application of the modulating method.

7. Claim 14, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino et al. (5,506,581) in view of Applicant Admitted Prior Art (AAPA) in further view of Kojima et al. (EP 0 779 623 A2).

Regarding to Claim 14, Ino discloses a data-modulating method and apparatus (Fig. 1) comprising an encoding circuit (Fig. 1, element 11), a pattern generating circuit (Fig. 1, element 12), pattern insertion circuit (Fig. 1, element 13), and a NRZI modulation circuit (Fig. 1, element 14), as described above. Ino further discloses, a data-demodulating method and apparatus (Fig. 5), comprising a decoding circuit (Fig. 5, element 23), a sync detection circuit (Fig. 5, element 24), and a pattern removal circuit (Fig. 5, element 22). However, Ino does not disclose the sync signal having six channel bits for identifying each sync signal.

The Applicant Admitted Prior Art (AAPA) discloses a data code satisfying the minimum and maximum run lengths depending on the RLL coding scheme further comprising code with six channel bits (Specification, Page 3, Table 1 "i = 2 & Specification, Page 4, lines 1-7 & Specification, Page 5, Table 2 "i = 2 & Specification, Page 6, lines 1-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing the sync pattern to contain six channel bits is a matter of design choice so as to provide a multiple of sync bits equal to the data train code bits, there is no criticality in selecting the sync pattern to have six channel bits, these could be selected depending on the application of the modulating apparatus. However, Ino in view of AAPA does not specify a data-providing medium for providing a data modulating/demodulating apparatus with a computer-readable program.

Kojima discloses a CPU (central processing unit) and a memory to be included in the synthesizing circuit (Page 4, lines 30-32 & Fig. 1, element 30). The CPU

implements an algorithm (Fig. 7) in the form of a computer program, while providing the sync pattern stored in the memory of the CPU. The CPU selects the stored pattern, which is optimum for the DC suppression from the memory as implemented in the algorithm. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the pattern generation circuit in Ino in view of AAPA can be implemented by a CPU and memory unit as described in Kojima. This would provide a more compact and flexible solution for varying the pattern generation and encoding algorithm depending on the information transmitting or recording the information on a recording medium, such as magnetic tape, optical disc.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (703) 305-0341. The examiner can normally be reached (Monday-Friday from 8:30 AM to 5:30 PM).

   If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (703) 305-4714.

   Any response to this action should be mailed to:

   Commissioner of Patents and Trademarks Washington, D.C. 20231

   Or faxed to:

   (703) 872-9314 (for Technology Center 2600 only)

   Hand-delivered responses should be brought to:

   Crystal Part II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600